

## CLAIMS:

1. A processing system comprising a plurality of processing element, the processing elements comprising a controller and computation means, the plurality of processing elements being dynamically reconfigurable as mutually independently operating task units which task units comprise one processing element or a cluster of two or more processing elements ,the processing elements within a cluster being arranged to execute instructions under a common thread of program control.
2. Processing system according to claim 1, wherein processing elements organized in a task unit share at least one common control signal for controlling instruction execution.
3. Processing system according to claim 2, wherein the common control signal is a flag controlling a guarded operation.
- 15 4. Processing system according to claim 3, wherein the guarded operation is a conditional jump.
5. Processing system according to any of the preceding claims, wherein the processing elements are connected to each other via data-path connections (DPC).
- 20 6. Processing system according to claim 5, wherein the data-path connections (DPC) are limited to neighbour-to-neighbour connections.
7. Processing system according to any of the preceding claims, wherein the common control signal is derived from intermediate control signals transmitted through a reconfigurable channel infrastructure connected to the processing elements.

8. Processing system according to claim 7, wherein the common control signal is derived by combining the intermediate control signals through a combination element associated to each processing element.

5 9. Processing system according to claim 8, wherein the combination elements consist of OR-gates.

10. Processing system according to claim 7, wherein the channel infrastructure comprises programmable sum-terms.

10 11. Processing system according to claim 7, wherein the channel infrastructure comprises programmable product-terms.

12. Processing system according to claim 7, wherein the channel infrastructure 15 comprises mutually transverse chains.

13. Processing system according to claim 12, wherein the intermediate control signals transmitted through chains having a first orientation are forwarded to the combination elements in chains having a second orientation.

20 14. Processing system according to claims 13, wherein the intermediate control signals transmitted through the chains having the second orientation are forwarded to the combination elements in the chains having the first orientation.

25 15. Processing system according to claims 7 or 12, wherein the channel infrastructure comprises combination elements for combining an intermediate control signal transmitted through the channel infrastructure with an operation control signal of associated processing elements, and programmable switches between pairs of processing elements, for locally controllably inhibiting transmission of intermediate control signals.

30 16. Processing system according to claim 15, wherein the combination elements consist of OR-gates.

17. Processing system according to claim 15, wherein the programmable switches comprise AND-gates.

18. Processing system according to claims 15, 16, or 17, wherein the  
5 programmable switches are programmed by signals stored in memory cells.

19. Processing system according to claim 18, wherein at least one of the processing elements can write to at least one of the memory cells.

10 20. Processing system according to claim 18, wherein a set of memory cells used to program the switches is organized as a data-word in a memory.

15 21. Processing system according to claim 20, wherein the memory contains multiple data-words, and wherein the programmable switches are programmed by selecting one of these data-words.

20 22. Processing system according to claims 21, wherein one or more of the processing elements can program the programmable switches by dynamically selecting the data-word in memory.

23. Processing system according to claims 18, 19, 20, 21, or 22, the memory consisting of volatile random access memory (RAM).

24. Processing system according to any of the preceding claims, wherein the  
25 processing elements comprise VLIW processors.

25. Processing system according to claim 24, wherein the VLIW processors comprise an internal interconnect network (IN).

30 26. Processing system according to claim 25, wherein the interconnect network (IN) consists of point-to-point connections.

27. Processing system according to claims 25 or 26, wherein the interconnect network (IN) comprises data-path connections (DPC) going across processing elements.

28. Processing system according to any of the preceding claims, wherein the processing elements are arranged in a 2-dimensional grid.

5 29. Method for operating a processing system comprising a plurality of processing elements, the processing elements comprising a controller and computation means, according to which method the plurality of processing elements are dynamically reconfigured as mutually independently operating task units, which task units comprise one processing element or a cluster of two or more processing elements, wherein the processing elements  
10 within a cluster execute instructions under a common thread of program control.